Refine Search

Search Results -

Term	Documents
(30 AND 6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	81
(L30 AND L6).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	81

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L31

Refine Search

Recall Text ⬌   Clear   Interrupt

Search History

DATE: Monday, October 24, 2005   Printable Copy   Create Case

Set Name side by side	Query	Hit Count	Set Name result set
*DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR*		
L31	L30 and l6	81	L31
L30	L25 and branch$5 near6 (predict$5 or guess$3 or speculat$5)	128	L30
L29	L25 and l6	147	L29
L28	L25 and l7	9	L28
L27	L25 and l8	0	L27
L26	L25 and l5	0	L26
L25	hardware near8 (multi or plur$7 or two or second or multipl$7) near5 thread$3	612	L25
L24	(thread$3 or multi near1 thread$3) and l1	0	L24
L23	L1 and (machine$1 or assembl$4 or compil$7or link$5)	1	L23
L22	L1 and assembl$4	0	L22
L21	L18 and l8	12	L21

L20	L18 and l7	2	L20
L19	L18 and l6	36	L19
L18	L17 and l5	40	L18
L17	(token$1 or value$1 or field$1 or flag$1 or bit$ or specif$5) near8 branch$5 near6 (predict$5 or guess$3 or speculat$5)	1464	L17
L16	l5 and l3	2	L16
L15	l5 and l2	2	L15

DB=PGPB,USPT; PLUR=YES; OP=OR

L14	l2 and l8	4	L14
L13	l2 and l7	2	L13
L12	l2 and l6	17	L12
L11	l5 and l8	17	L11
L10	l5 and l7	9	L10
L9	l5 and l6	92	L9
L8	(712/239)[CCLS]	421	L8
L7	(712/208-213, 233-240)![CCLS]	1366	L7
L6	(712/2-300)[CCLS]	11496	L6

DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR

L5	(number) near8 instruction$1 near8 (after or subsequent$2 or sequnc$3 or target) near8 branch$3 near8 execut$5	162	L5
L4	L3 not l2	4	L4
L3	(token$1 or value$1 or field$1 or flag$1 or bit$ or specif$5) near8 branch$5 near6 guess$3	28	L3
L2	(token$1 or value$1 or field$1 or flag$1 or bit$) near8 branch$5 near6 guess$3	24	L2

DB=USPT; PLUR=YES; OP=OR

L1	5724563.pn.	1	L1

END OF SEARCH HISTORY

IEEE Xplore· RELEASE 2.1

Welcome United States Patent and Trademark Office

BROWSE   SEARCH   IEEE XPLORE GUIDE

Search Results

Results for "((branch* <near/15> (speculat*, guess*, predict*) and number <near/5> instruction*)..."

Your search matched **20** of **1250969** documents.

A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

☑ e-mail

» Search Options

View Session History

New Search

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Modify Search

((branch* <near/15> (speculat*, guess*, predict*) and number <near/5> instruction ▶▶

☐ Check to search only within this results set

Display Format: ◉ Citation   ○ Citation & Abstract

Select   Article Information

☐   1. **Reducing the branch penalty in pipelined processors**
Lalja, D. J.;
Computer
Volume 21, Issue 7, July 1988 Page(s):47 - 55
Digital Object Identifier 10.1109/2.68

AbstractPlus | Full Text: PDF(780 KB)   IEEE JNL

☐   2. **SPARC64: a 64-b 64-active-instruction out-of-order-execution MCM processor**
Williams, T.; Patkar, N.; Shen, G.;
Solid-State Circuits, IEEE Journal of
Volume 30, Issue 11, Nov. 1995 Page(s):1215 - 1226
Digital Object Identifier 10.1109/4.475709

AbstractPlus | Full Text: PDF(1656 KB)   IEEE JNL

☐   3. **Control flow prediction schemes for wide-issue superscalar processors**
Dutta, S.; Franklin, M.;
Parallel and Distributed Systems, IEEE Transactions on
Volume 10, Issue 4, April 1999 Page(s):346 - 359
Digital Object Identifier 10.1109/71.762815

AbstractPlus | References | Full Text: PDF(716 KB)   IEEE JNL

☐   4. **Out-of-order commit processors**
Cristal, A.; Ortega, D.; Llosa, J.; Valero, M.;
High Performance Computer Architecture, 2004. HPCA-10. Proceedings. 10th International Sympo
14-18 Feb. 2004 Page(s):48 - 59
Digital Object Identifier 10.1109/HPCA.2004.10008

AbstractPlus | Full Text: PDF(320 KB)   IEEE CNF

☐   5. **FSEL - selective predicated execution for a configurable DSP core**
Panis, C.; Hirnschrott, U.; Krall, A.; Laure, G.; Lazian, W.; Nurmi, J.;
VLSI, 2004. Proceedings. IEEE Computer society Annual Symposium on
19-20 Feb. 2004 Page(s):317 - 320

AbstractPlus | Full Text: PDF(241 KB)   IEEE CNF

☐   6.
Memory reference reuse latency: Accelerated warmup for sampled microarchitecture simula
Haskins, J.W., Jr.; Skadron, K.;
Performance Analysis of Systems and Software, 2003. ISPASS. 2003 IEEE International Symposiu

6-8 March 2003 Page(s):195 - 203

AbstractPlus | Full Text: PDF(688 KB)   IEEE CNF

7. **Branch classification to control instruction fetch in simultaneous multithreaded architecture**
Knijnenburg, P.M.W.; Ramirez, A.; Latorre, F.; Larriba, J.; Valero, M.;
Innovative Architecture for Future Generation High-Performance Processors and Systems, 2002. Ir
on
10-11 Jan. 2002 Page(s):67 - 76
Digital Object Identifier 10.1109/IWIA.2002.1035020

AbstractPlus | Full Text: PDF(363 KB)   IEEE CNF

8. **Execution-based prediction using speculative slices**
Zilles, C.; Sohi, G.;
Computer Architecture, 2001. Proceedings. 28th Annual International Symposium on
30 June-4 July 2001 Page(s):2 - 13
Digital Object Identifier 10.1109/ISCA.2001.937426

AbstractPlus | Full Text: PDF(164 KB)   IEEE CNF

9. **Two cache lines prediction for a wide-issue micro-architecture**
Shu-Lin Hwang; Feipei Lai;
Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceedings. 6th Australasian
29-30 Jan. 2001 Page(s):71 - 79
Digital Object Identifier 10.1109/ACAC.2001.903361

AbstractPlus | Full Text: PDF(1032 KB)   IEEE CNF

10. **Instruction flow-based front-end throttling for power-aware high-performance processors**
Baniasadi, A.; Moshovos, A.;
Low Power Electronics and Design, International Symposium on, 2001.
6-7 Aug. 2001 Page(s):16 - 21
Digital Object Identifier 10.1109/LPE.2001.945365

AbstractPlus | Full Text: PDF(524 KB)   IEEE CNF

11. **Prediction and speculation techniques in ILP**
Mitrevski, P.; Gusev, M.; Misev, A.;
Information Technology Interfaces, 2000. ITI 2000. Proceedings of the 22nd International Conferen
13-16 June 2000 Page(s):67 - 72

AbstractPlus | Full Text: PDF(544 KB)   IEEE CNF

12. **Caching and predicting branch sequences for improved fetch effectiveness**
Onder, S.; Jun Xu; Gupta, R.;
Parallel Architectures and Compilation Techniques, 1999. Proceedings. 1999 International Confere
12-16 Oct. 1999 Page(s):294 - 302
Digital Object Identifier 10.1109/PACT.1999.807575

AbstractPlus | Full Text: PDF(244 KB)   IEEE CNF

13. **Improving trace cache effectiveness with branch promotion and trace packing**
Patel, S.J.; Evers, M.; Patt, Y.N.;
Computer Architecture, 1998. Proceedings. The 25th Annual International Symposium on
27 June-1 July 1998 Page(s):262 - 271
Digital Object Identifier 10.1109/ISCA.1998.694786

AbstractPlus | Full Text: PDF(92 KB)   IEEE CNF

14. **Control flow prediction with unbalanced tree-like subgraphs**
Toone, B.R.; Franklin, M.;
High Performance Computing, 1998. HIPC '98. 5th International Conference On
17-20 Dec. 1998 Page(s):221 - 227
Digital Object Identifier 10.1109/HIPC.1998.737992

AbstractPlus | Full Text: PDF(212 KB)   IEEE CNF

15. **Operating system impact on trace-driven simulation**
Casmira, J.; Fraser, J.; Kaeli, D.; Meleis, W.;
Simulation Symposium, 1998. Proceedings. 31st Annual
5-9 April 1998 Page(s):76 - 82
Digital Object Identifier 10.1109/SIMSYM.1998.668444

AbstractPlus | Full Text: PDF(160 KB)   IEEE CNF

16. **A study of tree-based control flow prediction schemes**
Cyril, B.; Franklin, M.;
High Performance Computing, 1997. Proceedings. Fourth International Conference on
18-21 Dec. 1997 Page(s):28 - 33
Digital Object Identifier 10.1109/HIPC.1997.634465

AbstractPlus | Full Text: PDF(516 KB)   IEEE CNF

17. **Control flow prediction with tree-like subgraphs for superscalar processors**
Dutta, S.; Franklin, M.;
Microarchitecture, 1995. Proceedings of the 28th Annual International Symposium on
29 Nov.-1 Dec. 1995 Page(s):258 - 263
Digital Object Identifier 10.1109/MICRO.1995.476834

AbstractPlus | Full Text: PDF(560 KB)   IEEE CNF

18. **Control flow prediction for dynamic ILP processors**
Pnevmatikatos, D.N.; Franklin, M.; Sohi, G.S.;
Microarchitecture, 1993. Proceedings of the 26th Annual International Symposium on
1-3 Dec. 1993 Page(s):153 - 163
Digital Object Identifier 10.1109/MICRO.1993.282747

AbstractPlus | Full Text: PDF(988 KB)   IEEE CNF

19. **The effect of speculative execution on cache performance**
Pierce, J.; Mudge, T.;
Parallel Processing Symposium, 1994. Proceedings., Eighth International
26-29 April 1994 Page(s):172 - 179
Digital Object Identifier 10.1109/IPPS.1994.288304

AbstractPlus | Full Text: PDF(676 KB)   IEEE CNF

20. **Guarded execution and branch prediction in dynamic ILP processors**
Pnevmatikatos, D.N.; Sohi, G.S.;
Computer Architecture, 1994. Proceedings the 21st Annual International Symposium on
18-21 April 1994 Page(s):120 - 129
Digital Object Identifier 10.1109/ISCA.1994.288156

AbstractPlus | Full Text: PDF(924 KB)   IEEE CNF

Help   Contact Us   Privac